IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 09/483,101
Filed: January 14, 2000
Inventor(s):
Kevin J. McGrath and Michael T. Clark

Title: Establishing an Operating Mode in a Processor

§ Examiner: Li, Aimee J.
§ Group/Art Unit: 2183
§ Atty. Dkt. No: 5500-54700

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Lawrence J. Merkel
Printed Name

Signature

August 28, 2003
Date

FEE AUTHORIZATION

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Respectfully submitted,

Lawrence J. Merkel
Reg. No. 41,191
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800
Date: August 28, 2003

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Signature

8/28/03
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APPEAL BRIEF

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Further to the Notice of Appeal filed August 7, 2003, Appellants present this Appeal Brief.

I. REAL PARTY IN INTEREST

The Real Party in Interest in the present appeal is Advanced Micro Devices, Inc., the assignee, as recorded at Reel 010509, Frame 0421.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to Appellants, Appellants' legal representatives, or assignee which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-10 and 17-22 are pending in the present application. Claims 1 and 17 were rejected under 35 U.S.C. § 102(b) as being unpatentable over James L. Turley's

Advanced 80386 Programming Techniques ("Turley"). Claims 2-10 and 18-22 were objected to as being dependent from a rejected base claim but would be allowable if rewritten in independent form. **Since the record shows that claims 2-10 and 18-22 recite patentable subject matter, these claims are not on appeal and are not included in the attached Appendix. However, claims 2-10 and 18-22 remain pending in the application.** A copy of claims 1 and 17 on appeal is included in the attached Appendix.

IV. STATUS OF AMENDMENTS

There are no outstanding unentered amendments in the present application.

V. SUMMARY OF THE INVENTION

In various embodiments, a processor (10) may include a segment register (24A) and a control register (26). The segment register may be configured to store a segment selector (24AA) identifying a segment descriptor (40, 54) including a first operating mode indication (42), a second operating mode indication (44), and one or more bits identifying a segment described by said segment descriptor as a code segment (52). The control register may be configured to store an enable indication (LME). The processor may be configured to establish a default address size responsive to the enable indication, the first operating mode indication, and the second operating mode indication (see, e.g., Figs. 1-3 and 5-6; see also the specification, page 6, lines 13-20; page 7, lines 22-28; page 8 lines 18-28; and page 18, line 15-page 20, line 28).

In some embodiments, the processor may support default address sizes greater than 32 bits in various modes, while supporting compatibility modes for 32 and 16 bit processing. Additionally, legacy 16 bit and 32 bit modes may be supported (see, e.g., specification, page 2, line 5-page 3, line 10).

VI. ISSUES

A. Whether claims 1 and 17 are patentable under 35 U.S.C. § 102(b) over Turley.

VII. GROUPING OF CLAIMS

For purposes of the issues set forth in Section VI of this Appeal Brief only, the claims may be grouped as follows:

Claim 1 stands or falls alone.

Claim 17 stands or falls alone.

Appellants submit that each pending claim is independently patentable.

VIII. ARGUMENT

A. Rejection of Claims 1 and 17 Under 35 U.S.C. § 102(b) over Turley

Claim 1

Appellants respectfully submit that claim 1 recites a combination of features not taught or suggested in Turley. For example, claim 1 recites a combination of features including: "a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication, a second operating mode indication, and one or more bits identifying a segment described by said segment descriptor as a code segment; a control register configured to store an enable indication, wherein said processor is configured to establish a default address size responsive to said enable indication, said first operating mode indication, and said second operating mode indication". Turley does not teach or suggest the above highlighted features.

The Final Office Action mailed May 5, 2003 in the present application ("Final Office Action"), in the Response to Arguments Section, alleges that the first operating mode indication is anticipated by Turley's privilege level (DPL) and that the second operating mode indication is anticipated by Turley's granularity bit (G). (See Final Office Action, page 4, item 9). Appellants respectfully disagree.

With regard to the privilege level (DPL), Appellants respectfully submit that Turley has no teaching or suggestion that the DPL is in any way related to default address size. Turley teaches: "This 2-bit field indicates the level of privilege associated with the memory space that the descriptor defines. DPL 0 is most privileged, and DPL 3 the least" (Turley, page 51, paragraph 5). Additionally, Turley teaches the following with regard to privilege level: "Working closely with memory management is a relatively new system of privileged checking...with this method, every piece of code and data is assigned one of four privilege levels, and the processor automatically performs privilege validation on every memory cycle. If the application is privileged enough, its memory access will be granted. If not, the processor will deny access and generate a privilege fault; the operating system will then take over." (Turley, page 10, last paragraph continuing on to page 11). Thus, the privilege level may be used in determining if a memory access is granted or denied. Applicants respectfully submit that there is no teaching or suggestion in Turley that the privilege level is a first operating mode indication "wherein said processor is configured to *establish a default address size* responsive to said enable indication, *said first operating mode indication*, and said second operating mode indication".

Notably, the Advisory Action mailed June 12, 2003 ("Advisory Action") in the above application did not address the above argument. Appellants respectfully submit that, since the DPL does not teach the first operating mode indication, the rejection fails for at least this reason.

Furthermore, Turley teaches the following regarding the granularity (G) bit: "When this bit is cleared, the 20-bit limit field is assumed to be measured in units of 1 byte. If it is set, the limit field is in units of 4096 bytes" (Turley, page 52, third paragraph). Turley further teaches: "The granularity bit allows you to build a segment larger than 1 MB." (Turley, page 54, second paragraph). Thus, the granularity bit, in conjunction with the limit field, defines the size of a segment. This does not teach or suggest a second operating mode indication "wherein said processor is configured to

establish a default address size responsive to said enable indication, said first operating mode indication, and *said second operating mode indication*".

The Advisory Action alleges that the G bit "determines whether the address size is measured in 1 byts [sic] or 4096 bytes. This is the value of the default offset address size. It determines how large the default offset address is." (See Advisory Action, continuation sheet, first paragraph). Turley does not support these allegations. The G bit determines how to interpret the limit field, and defines the size of the segment. Addresses of the default address size (which is NOT determined by the G bit) would be used to address the segment, independent of the value of the G bit.

The last sentence of item 9 in the Final Office Action states that "Applicants admit in their argument that there is an enable indication for the default address size". The Advisory Action states that "Applicants have admitted that the D bit, or enable indication, deals with the default address size" (See Advisory Action, continuation sheet, last paragraph). Applicants respectfully disagree with the alleged admission. Nothing in Applicants' remarks is an admission as alleged in the Final Office Action and the Advisory Action. The mere statement that the D bit may have be related to address size is NOT an admission that the D bit is the claimed enable indication: "a control register configured to store an enable indication".

The rejection of claim 1 in the Final Office Action also refers to various portions of Turley more generally. More particularly, the Final Office Action alleges that Turley teaches the first and second operating mode indications at page 49, table: A segment descriptor; pages 50-54; and page 57 (See Final Office Action, page 2, item 5a). With such general recitations of teachings, it is unclear exactly what in Turley's segment descriptor is alleged to be the first and second operating mode indications. However, the table labeled "A segment descriptor" on page 49 merely generally describes a segment descriptor, and offers no details. Pages 50-54 describe a segment descriptor in more detail, and describe the various bits. Page 57 describes the use of the D bit and the G bit for stack and data segments. Nothing in the description of Turley's segment descriptor

indicates that Turley's segment descriptor includes a first operating mode indication and a second operating mode indication as recited in claim 1. The Final Office Action also refers to page 178, paragraphs 2 and 3 of Turley. This section of Turley describes the use of task state segments (TSS), and appears to have nothing to do with the above highlighted features of claim 1.

Accordingly, Appellants respectfully submit that claim 1 is patentable over Turley for at least the above stated reasons. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 1 over Turley is in error and request reversal of the rejection.

Claim 17

Appellants respectfully submit that claim 17 recites a combination of features not taught or suggested in Turley. For example, claim 17 recites a combination of features including: "establishing a default address size in a processor in response to an enable indication in a control register within said processor, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor, said segment descriptor further including one or more bits identifying a segment described by said segment descriptor as a code segment".

The Final Office Action relies on the same teachings from Turley to allegedly teach the first and second operating modes in claim 17 as were relied on for claim 1 (namely, the DPL, the G bit, page 49, table: A segment descriptor; pages 50-54; and page 57). These teachings, highlighted above with regard to claim 1, also do not teach or suggest the first operating mode indication and the second operating mode indication recited in claim 17.

Additionally, the Final Office Action cites Turley's page 176, paragraph 1 and page 178, paragraphs 2-3 with regard to "in response to an enable indication in a control register within said processor" as recited in claim 17. However, page 176, paragraph 1 and page 178, paragraphs 2-3 describe the task state segment (TSS) and how it can be

used for task switching. This has nothing to do with the above highlighted features, nor "establishing a default address size in a processor in response to an enable indication in a control register within said processor..." as recited in claim 17.

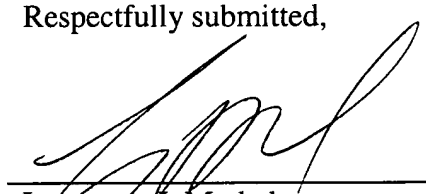
Accordingly, Appellants respectfully submit that claim 17 is patentable over Turley for at least the above stated reasons. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 17 over Turley is in error and request reversal of the rejection.

IX. CONCLUSION

For at least the foregoing reasons, Appellants respectfully submit that the Examiner's rejections of claims 1 and 17 were erroneous and respectfully request that the Board of Patent Appeals reverse the Examiner's rejections.

A Fee Authorization Form authorizing a deposit account charge for the fee for filing an appeal brief under 37 C.F.R. § 1.17(c) is enclosed. If the fee is missing or insufficient, or if any other fees are due, the Commissioner is authorized to charge said fees to Deposit Account No. 501505/5500-54700/LJM.

Respectfully submitted,



Lawrence J. Merkel
Reg. No. 41,191
AGENT FOR APPELLANT(S)

Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 476-1400

Date: 8/28/03

X. APPENDIX

This appendix includes a copy of the claims involved in this appeal.

1. A processor comprising:

a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication, a second operating mode indication, and one or more bits identifying a segment described by said segment descriptor as a code segment;

a control register configured to store an enable indication, wherein said processor is configured to establish a default address size responsive to said enable indication, said first operating mode indication, and said second operating mode indication.

17. A method comprising:

establishing a default address size in a processor in response to an enable indication in a control register within said processor, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor, said segment descriptor further including one or more bits identifying a segment described by said segment descriptor as a code segment; and

generating addresses of said default address size.